Center For Development Of Advanced Computing
Vellayambalam
Thiruvananthapuram
Kerala State, PIN Code: 695033, India
Phone No- (0471) 2721067/ 2723333 Fax - (0471) – 2721067
Email: madhavan@cdactvm.in
http://www.cdactvm.in

TENDER

Tender . No.PHS.RD. HDG 063D .ENQF. 661 .08-09 Date: 08.12.08

Due on : 23.12.08

EDA tools for ASIC and Custom IC Design as per the following detailed specifications.

Make: M/s Cadence Design Systems / M/s Synopsys/ M/s Magma Design Automation

EDA TOOL SPECIFICATION FOR ASIC AND CUSTOM IC DESIGN

- EDA tools for **low power digital and mixed signal design** for technology node up to 90nm.
- Tools to run on SUN Solaris -10(64 bit) with **multicore multithreading** feature.
- Major foundries including **TSMC, UMC, Chartered Semi, SMIC, IBM, AustriaMicroSystems** etc. should be supported for **Reference flow** and **Process Design Kit (PDK).**
- License options: **floating, perpetual** with **parallel processing and multithreading support.**
  Optional: Above with **time based license** for 3 years
- Training for the full tool chain should be provided at CDAC, Trivandrum

- **Low Power implementation Support**
  The entire tool chain should support all major low power implementation techniques in the industry with following features.
  - Clock gating and operand isolation as a part of synthesis.
  - Multi supply, voltage island implementation, and power analysis.
  - CPF or UPF.
  - Power shut off to reduce leakage power.

- DVFS.
- Power aware placement and routing.

- **Simulator**

  Tool to simulate and verify the design, and to ensure that it is logically correct without major timing errors.

  Tool should support:

  - Complete verification process from planning to closure.
  - Automatic deployment and management of verification jobs.
  - Low power simulation with CPF or UPF.
  - VHDL, Verilog, System Verilog, System C, etc.
  - Assertion based verification
  - Coverage analysis including functional, HDL & assertion coverage
  - HDL linting.
  - Sign-off quality for all major foundries
  - Capability for analysis, source browsing, transaction and waveform viewing.
  - Multi-million gate (> 50M) capacity for large designs

- **RTL Synthesis**

  Synthesis tool translates the RTL description to a technology independent netlist and then optimizes to a target technology constrained to timing, area, power and test requirements.

  Tool should support:

  - Multi-million (> 50M) gate top-down compilation of VHDL, Verilog, System Verilog.
  - SDC and TCL based constraints.
  - Test insertion and scan stitching.
  - Data path and arithmetic optimization.
  - Testability rule analysis and fixing.
  - Should offer more flexibility for users to control optimization on specific areas of design.
  - Integrated STA, test synthesis and power synthesis.
  - Accurate congestion prediction in synthesis.
  - Synthesize netlist based on actual layout parameters apart from wireload model estimation.
  - Optimize for timing (including TNS and WNS), power (static and dynamic) & area concurrently.
  - Multi-Vt leakage power optimization, hierarchical and multi stage clock gating & operand isolation.
  - CPF or UPF.
  - Synthesis support for power-shut off with isolation and state retention.
  - Top-down register re-timing.
  - Top-down multi-supply voltage synthesis.

- **DFT**

  Tool to insert testability features to the design to validate that the product hardware contains no defects that could, otherwise, adversely affect the product's correct functioning.

  Tool should support:

  - All industry standard DFT methodologies.
  - Automatic insertion and wiring of DFT Functions (control, scan, I/O, testpoint)
  - Rigorous and extensible DFT analysis and verification (scan, BIST, 1149.1).
  - Automatic Test Pattern Generation capability.
  - Testing of embedded IP cores.
  - Memory BIST capability (macro generation).
  - Test data compression.
  - Logic level fault isolation.

- Defect oriented fault modeling capability
- Check testability of the design at the pre-synthesis stage (RTL)

.

- **Floor planning, Prototyping, Power planning**

  The tool places hierarchical modules and macros meeting various design constraints, ensuring proper power distribution for cells & macros.

  Tool should support:

- Multi-million gate capacity for large designs.
- Automatic floor plan size estimation and macro placement subject to design constraints.
- Relative floor planning for ECO.
- Flip-chip bump placement, BGA routing etc.
- Timing budgeting and partitioning for hierarchical designs.
- Automated power planning and routing with wire editing.
- Automatic implementation quality macro placements considering all possibilities in the floor plan
- Support to prototype, macro place, pin optimize large designs.
- Reshaping of blocks to maximize the area utilization and routability.
- Concurrent hierarchical design.
- Timing driven automatic macro placement.
- Early analysis and feasibility exploration capabilities
- Power network analysis, power network synthesis and power pad synthesis.
- High quality dynamic and leakage optimization.
- Power aware placement technology.
- TCL script.
- Inputs:
    a. Verilog netlist
    b. .lib, lef, technology file (.tf) etc.
    c. SDC, DEF, SPEF etc.
- Outputs:
    a. Verilog netlist
    b. SDC, DEF, SPEF etc.
    c. GDSII

- **Physical Optimization,CTS,Routing**

  The tool optimizes the design for constraints in terms of area, power and timing along with clock tree insertion and signal routing.

  Tool should support:

  - Optimization of timing, area, and power in a comprehensive way.
  - Multi mode multi corner timing analysis and optimization.
  - Optimization for crosstalk and OCV
  - CTS (automatic and manual) with support for low power and multiple clock domains
  - Timing optimization should be available at various stages of design flow such as placement, CTS, routing etc.
  - Complex clock gating in clock tree synthesis.
  - Low power, SI aware CTS.
  - CTS skew and latency analysis.
  - The physical implementation tool should have tight correlation with the synthesizer.
  - TCL script.
  - Analysis WNS, congestion, cell density, power etc.

- **ECO Placement & ECO Routing**

  The process of inserting a logic change directly into the netlist after it has already been processed by an automatic tool to save time, by avoiding the need for full ASIC logic synthesis, place, route, layout extraction, and timing verification

  Tool should support:

  - ECO with register changes, RTL changes, netlist changes.
  - ECO that includes only combinational logic.
  - Support to map/place/route ECO cells based on timing, minimum wire lengths & DRCs.
  - TCL script.

- **Formal Verification**

  The tool is to prove the correctness of a circuit implementation with respect to its specification by avoiding the verification by exhaustive simulation, which is time consuming.

  Tool should support:

  - Functional equivalence of a design at various stages from RTL to layout. (Front-end, back-end, ECO, Full Chip etc.)
  - Functional correctness of design after resource sharing, register retiming, operator merging and optimization for low power implementation.
  - Logic equivalence checking for complex low power SOC
  - Functional and structural checks for low power designs.
  - Graphical debugging.
  - Clock domain crossing and semantics check.
  - Should report power and ground domain assignment related problems and floating connections.
  - Missing, redundant, wrong domain location or wrong connectivity of level shifters and isolation cells reporting.
  - Incorrect power and ground connectivity, including shorts and opens reporting.
  - Report instances with undefined power domains, or mixed power domains
  - Missing, redundant, incorrect power connection, wrong level shifter type reporting.
  - Missing, redundant, incorrect isolation cell power connectivity reporting.
  - Reporting of power control signals to power switches, isolation cells, state retention that is not powered.
  - Reporting incorrect power connection to state retention registers.

- **Sign Off Timing Analysis**

  The Sign off timing analyzer checks whether the desired timing is valid for the layout, which is performed after placement of cells, clock tree insertion and routing of wires, considering the delay due to the parasitics of the interconnect.

  Tool should support:

  - Sign off quality timer engine.
  - SDC and other constraining formats.
  - Multi mode multi corner analysis.
  - Accurate SI and IR drop analysis and its impact on both timing and functionality.
  - Integrated tape-out proven delay calculator

- On-the-fly path simulation of critical path with additional feature for analyzing the impact of crosstalk and IR drop along the path.
- CPF or UPF.
- Static and dynamic IR drops should be considered for path delays and SI.

- **Power Analysis**

  To analyze the power consumption of the design considering both static and dynamic drop along with low power implementation techniques.

  Tool should support:

- Accurate hierarchical power estimation
- Drop-aware timing and SI noise analysis.
- Analysis of static and dynamic power consumption of cells and macros.
- Static and dynamic power rail analysis
- Multiple voltage domains, multiple thresholds, level shifting logic, voltage clamp circuitry and power switch to reduce leakage current.
- Signal electro migration analysis and repair.

- **Sign off Parasitic Extraction**

  The tool is to extract the 3D parasitics of the layout for the computation of the delay time introduced due to parasitics.

  Tool should support:

- 3D parasitic extractor, of Sign-off quality for all major foundries.
- Unlimited parasitic (RCLK) extraction capability.
- Cell-level and transistor-level extraction
- Integrated substrate extraction modeling capabilities
- Multi-corner extraction in single run.
- Incremental extraction.
- Hierarchical extraction for full-chip capacity.
- Various file formats like GDS II, LEF/DEF, CDBA, and OA etc.
- Should generate a circuit-level schematic with the parasitics included

- **Sign off DRC – LVS**

  The tool is to do the design rule checks and layout v/s schematic checks.

  Tool should support:

- Recognition of generic devices prevalent in analog-CMOS, bipolar, diodes etc.
- Nets mismatch, Devices mismatch, Pins mismatch, Parameters mismatch

- Debug LVS issues with cross probing of layout and schematic simultaneously.
- Proven at major foundries worldwide with fully qualified run sets available.
- Full set of geometric processing capabilities.

➢ **Full-custom Layout**

- Full Custom Layout Editor
- Automated device editing, including abutment, pin permutation, folding, chaining, and cloning
- Design-rule–driven editing with real-time notification or enforcement of process rules
- Dynamic measurement
- Constraint-driven specification, management, and real-time notification or enforcement"
- Design-rule–driven interactive routing
- ECO support
- Cross-probing and annotation to schematics
- Move, copy, stretch, rotate, and delete editing options

➢ **Analog Simulator**

- Waveform viewer with calculator and Analyzing tool
- Schematic entry of the design should be supported
- MOSFET models, including BSIM 1, 2, 3 and 4,HVMOS, SOI
- BJT Models -Gummel-Poon models, HBT, VBIC
- Diode models level 1,2, and 3, JFET, and GaAS MESFET models
- DC, AC, and transient analysis Noise, transfer function, and sensitivity analysis, Transient noise analysis
- Simulator should support multi threading.
- Should support exploration of effects such as electromigration, IR drop, signal integrity and substrate degradation.
- Full chip simulator without compromising on speed and accuracy.
- Post layout verification, Reliability analysis, Custom digital verification

➢ **Analog and Mixed Signal Design**

- Single executable mixed-signal/mixed language simulator
- Schematic entry of the design should be supported.
- Integration with LVS, DRC and extraction tools
- Full chip timing analysis capability
- Common mixed-signal waveform database
- Should accept Verilog-AMS, VHDL-AMS, Verilog, VHDL, and Spectre.
- Should support industry standard netlist formats SPICE, Spectre, HSPICE, SystemC, SystemVerilog