

32-bit RISC Processor for System-on-Chip Implementations

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Agenda

- Introduction to SoC
- Advantages of IP-Cores
- 32-bit RISC processor
- Co-processor
- AMBA Architecture
- Cache Architecture & Organisation
- MMU Architecture & Translations
- ER902 based SoC Solutions

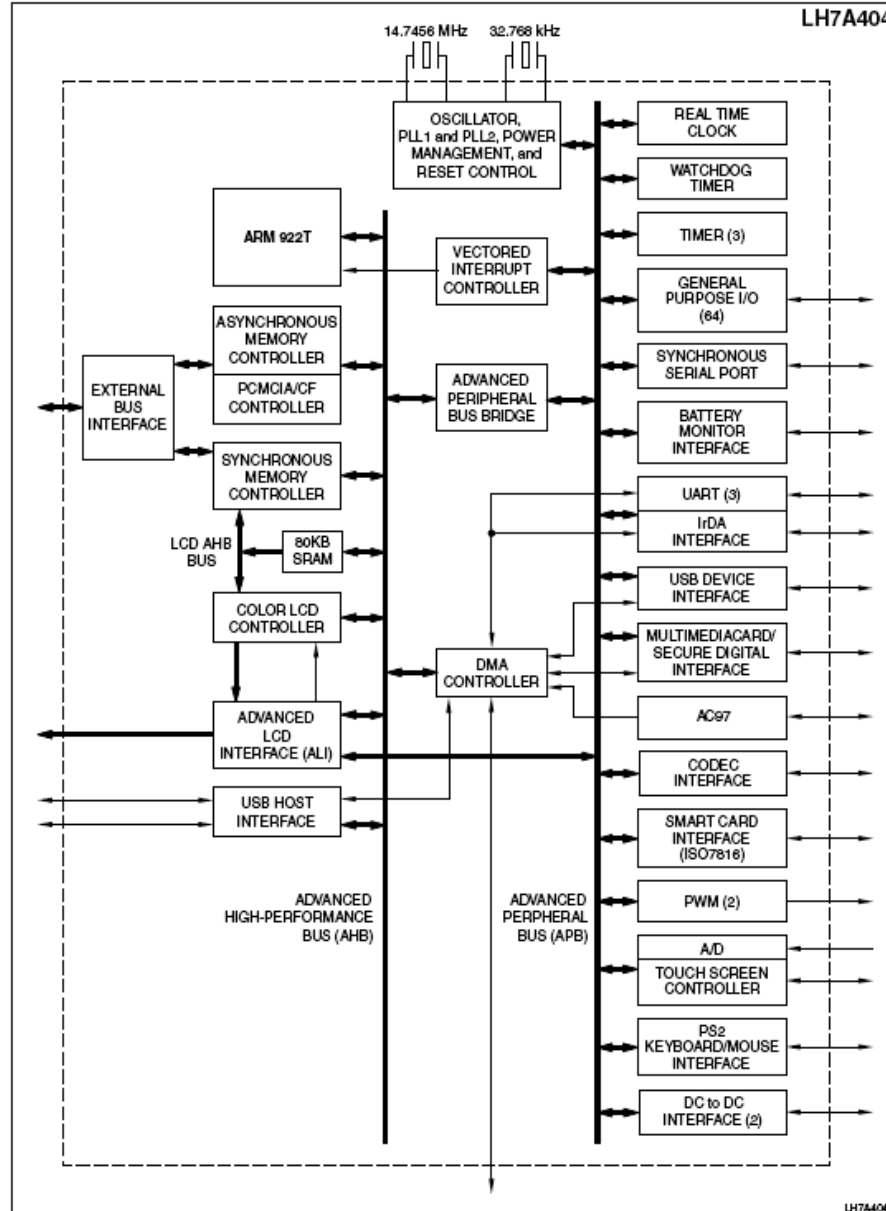
Introduction

- Portable electronic devices require power efficient and small footprint systems.
- Single chip or System-on-Chip solutions hold the key to achieve these requirements.

System-on-Chip

- ❖ Integrates all components of an electronic system into a single chip.
- ❖ It may contain digital, analog, mixed-signal functions

A typical SoC with embedded MCU



Advantages of IP-Cores

- Pre-designed, pre-verified building blocks
- Re-configurability
- Reusable modules to build SoC solutions as per customer requirements
- Less time required to deliver products

C-DAC(T)'s Initiative

- Hardware Design Group has developed a wide range of synthesisable technology independent IP cores under the brand name *ASTRA*
- *ASTRA* will form a basic building block in any SoC implementation

ASTRA- Portfolio of IP

Processor

- ER902: 32-bit RISC Processor
- ER8051: 8-bit microcontroller compatible with Intel 8051 family
- ER8085: 8-bit microprocessor compatible with Intel 8085
- ER9101: 16-bit Bit Slice ALU

Peripherals

- ERRTC: Real Time Clock
- ERTIMER: 32-bit configurable timer
- ERDMA: 8237 compatible DMA controller
- ER15530: Manchester Encoder Decoder

ASTRA- Portfolio of IP

Communication

- ER16450: UART compatible with NS16450
- ERUSB2: USB 2.0 Device Controller
- ERMAC: IEEE802.3 compliant Media Access Controller
- EROTG: USB On The Go Controller

Mixed Signal

- Sigma-Delta ADC

ASTRA- Deliverables

- VHDL source code
- Technology specific netlist
- Core specification
- Verification suite
- Technical Documentation

32-bit RISC Processor

Two variants of our Processor

ER902

- Basic Processing Unit
- AMBA Interface

ER922

- ER902
- Cache & MMU
- External Co-processor Support
- AMBA Interface

32-bit RISC Processors (contd..)

Architectural features

- Harvard architecture
- 32-bit data/address bus
- 5 stage pipelined architecture
- Load/Store architecture
- Data processing operations only on register contents
- Uniform and fixed length instruction fields

Instruction set

- All instructions are executed conditionally
- All are single word instructions
- Instructions may be broadly divided into :
 - Branch Instructions
 - Data Processing Instructions
 - Status Register Transfer Instructions
 - Load and Store Instructions
 - Coprocessor Instructions
 - Exception Generating Instructions

Register File

- 31 General Purpose and 6 Program Status Registers, each 32-bit long
- Only 16 General Purpose Registers and 1 or 2 Status Registers are visible at a time
- R15 and R14 are used as Program Counter and link Register respectively
- Visibility of registers depends on the following seven processor modes:

Processor Modes

1. User mode
2. System mode
3. IRQ mode
4. FIQ mode
5. Supervisor mode
6. Abort mode
7. Undefined mode

General purpose registers may be :

- Unbanked (R0 – R7)
- Banked (R8 – R14)
- R15, the program counter

Status Registers:

- Unbanked (CPSR – Current Program Status Register)
- Banked (SPSR – Saved Program Status Register)

Modes

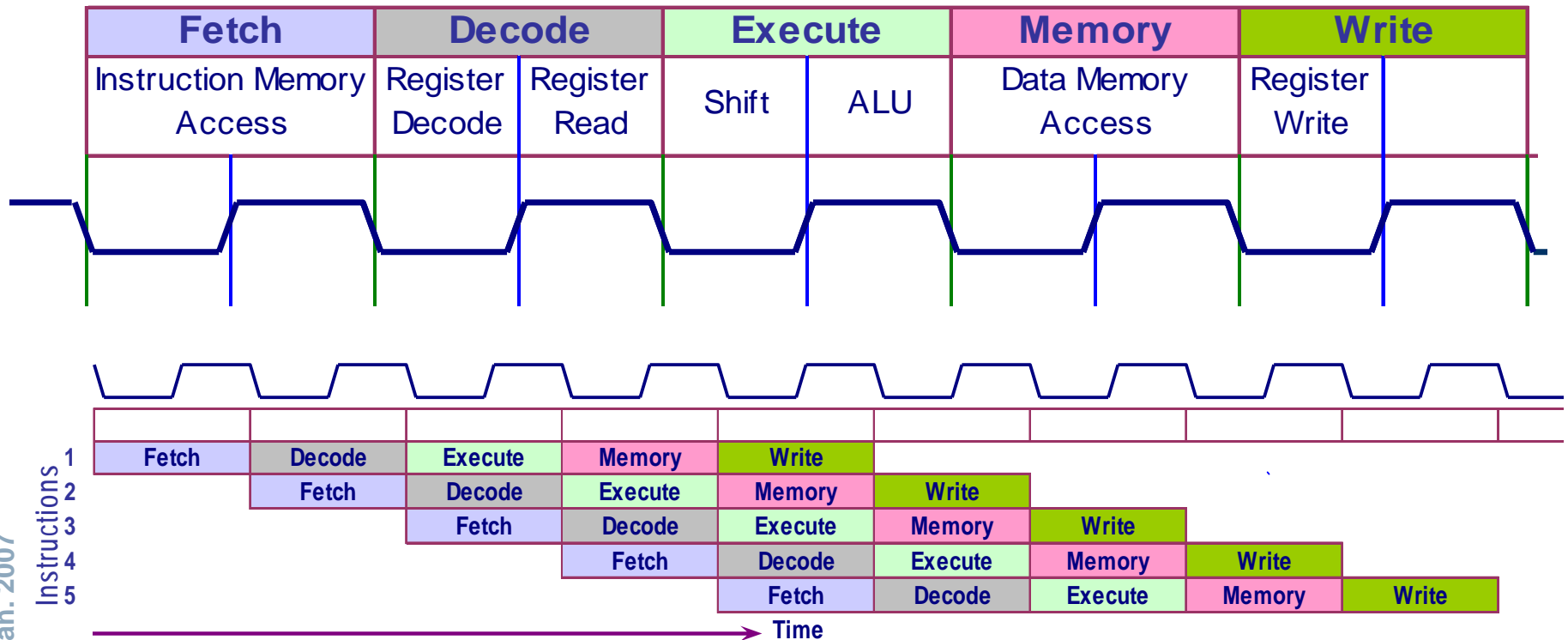
Privileged Modes

Exception Modes

USER	SYSTEM	SUPERVISOR	ABORT	UNDEFINED	INTERRUPT	FAST INTERRUPT
R0	R0	R0	R0	R0	R0	R0
R1	R1	R1	R1	R1	R1	R1
R2	R2	R2	R2	R2	R2	R2
R3	R3	R3	R3	R3	R3	R3
R4	R4	R4	R4	R4	R4	R4
R5	R5	R5	R5	R5	R5	R5
R6	R6	R6	R6	R6	R6	R6
R7	R7	R7	R7	R7	R7	R7
R8	R8	R8	R8	R8	R8	R8_fiq
R9	R9	R9	R9	R9	R9	R9_fiq
R10	R10	R10	R10	R10	R10	R10_fiq
R11	R11	R11	R11	R11	R11	R11_fiq
R12	R12	R12	R12	R12	R12	R12_fiq
R13	R13	R13_svc	R13_abt	R13_und	R13_irq	R13_fiq
R14	R14	R14_svc	R14_abt	R14_und	R14_irq	R14_fiq
PC	PC	PC	PC	PC	PC	PC
CPSR	CPSR	CPSR	CPSR	CPSR	CPSR	CPSR
		SPSR_svc	SPSR_abt	SPSR_und	SPSR_irq	SPSR_fiq

Pipeline Implementation

- Five stage pipeline is implemented, the stages being: Fetch, Decode, Execute, Memory, Write



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Co-processors

A special-purpose processing unit that assists the processor in performing certain types of operations.

For example, a DSP coprocessor performs mathematical computations like floating-point operations and DSP functions.

- Up to 16 coprocessors can be connected to the Processor core at a time
- It is specified with numbers 0 to 15 in coprocessor instructions
- Coprocessor 15 (CP15) is the system control coprocessor used to control Cache, MMU operations.

Advanced Microcontroller Bus Architecture (AMBA)

- AMBA specification defines an on-chip communication standard for designing high performance embedded microcontrollers
- Initiated and Driven By **ARM**

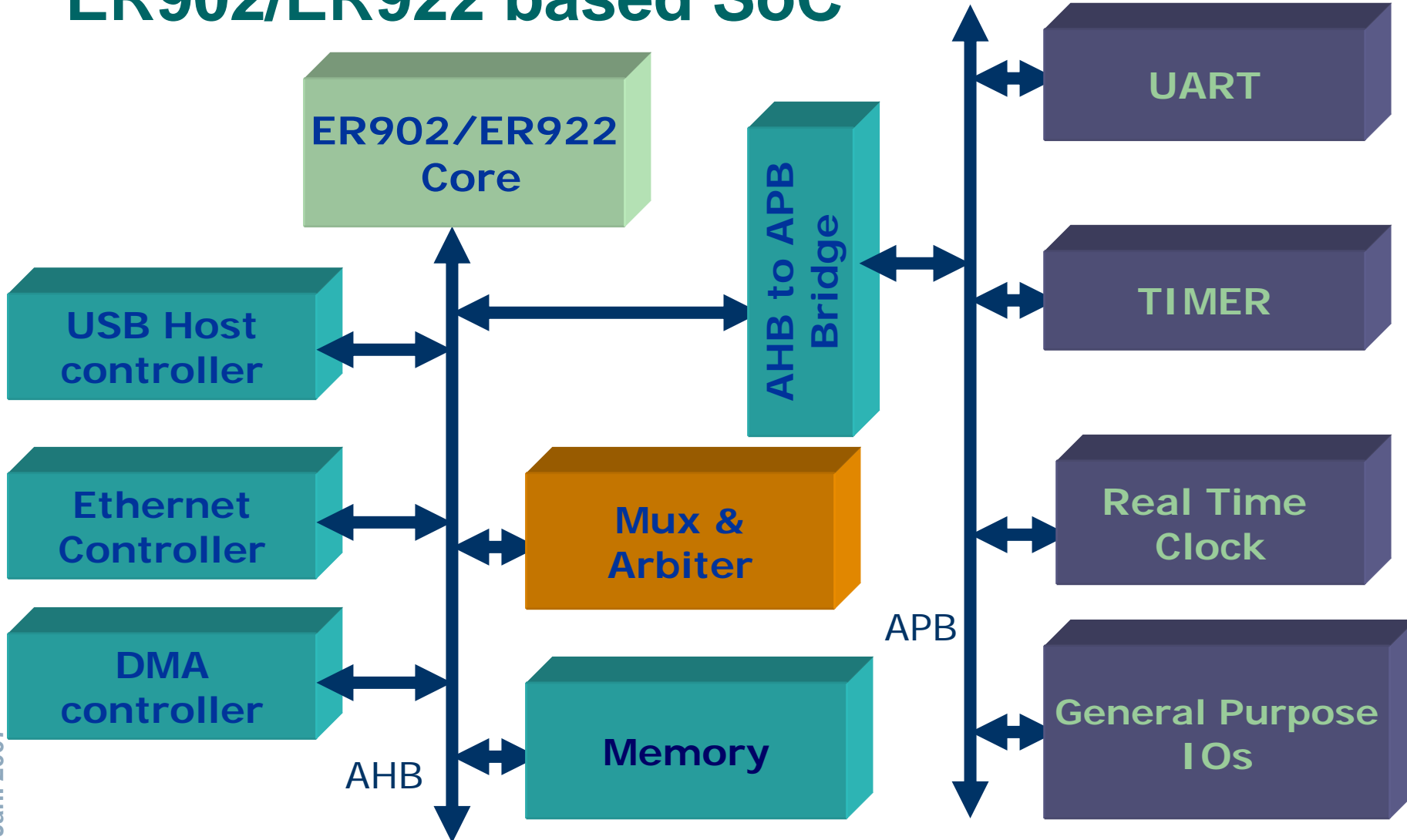
AMBA mainly consists of three type of Buses

AHB (Advanced High Performance Bus)

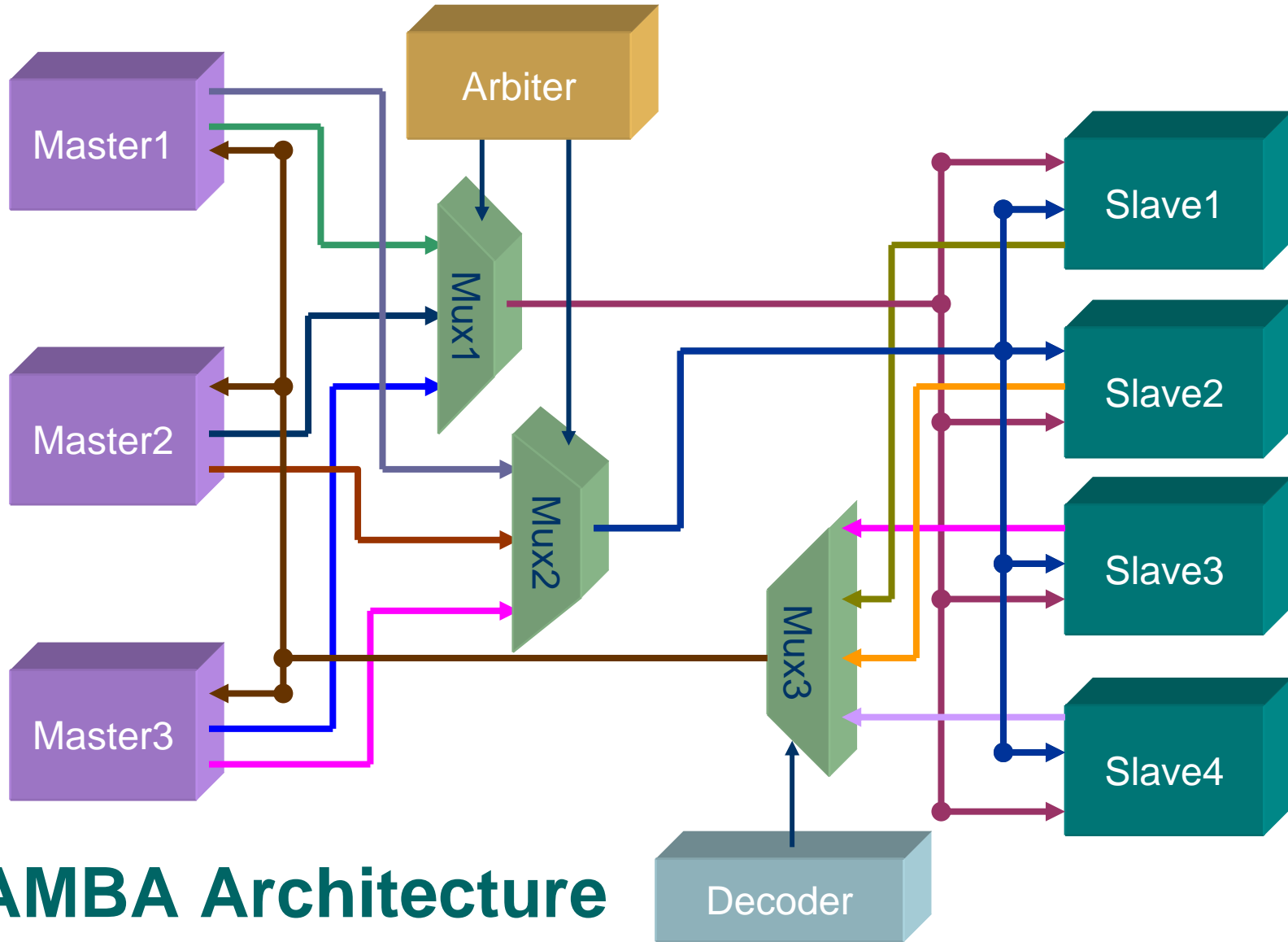
ASB (Advanced System Bus)

APB (Advanced Peripheral Bus)

ER902/ER922 based SoC



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AMBA Architecture

AMBA (contd..)

Advanced High-performance Bus (AHB)

- Intended to address the requirements of high-performance designs
- Supports Multiple Masters
- Pipelined operation
- Burst Operations

Advanced Peripheral Bus (APB)

- To interface low bandwidth peripherals which do not require the high performance
- Simple Interface
- Latched Address and Control signals

Cache & MMU

In order to achieve full performance and multi tasking in RTOS, the processor should support Cache and MMU.

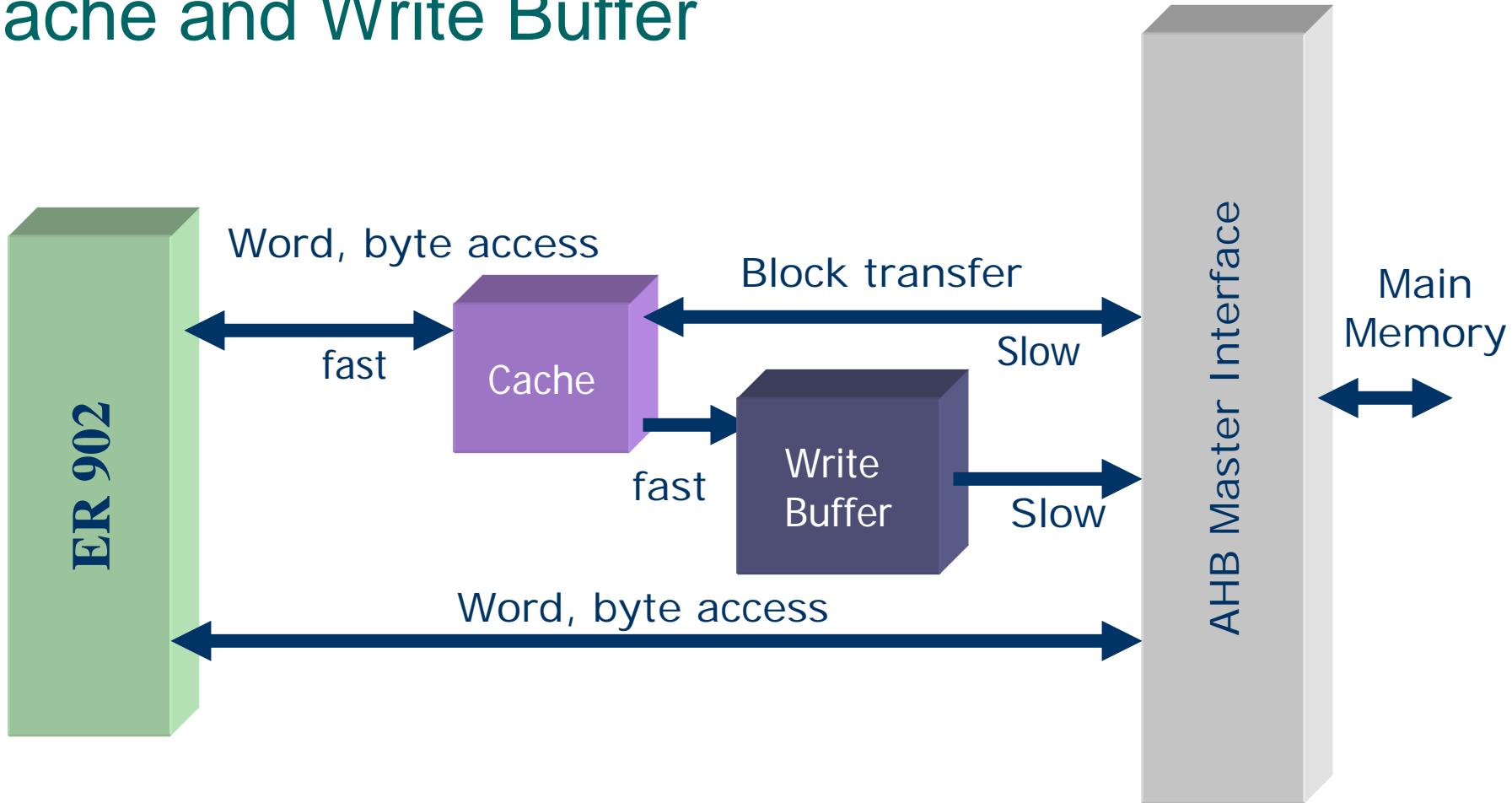
Cache

- 8KB instruction and 8KB data cache
- 64-way set associative cache with CAM implementation.
- 8 words per line
- Pseudo random or Round robin replacement

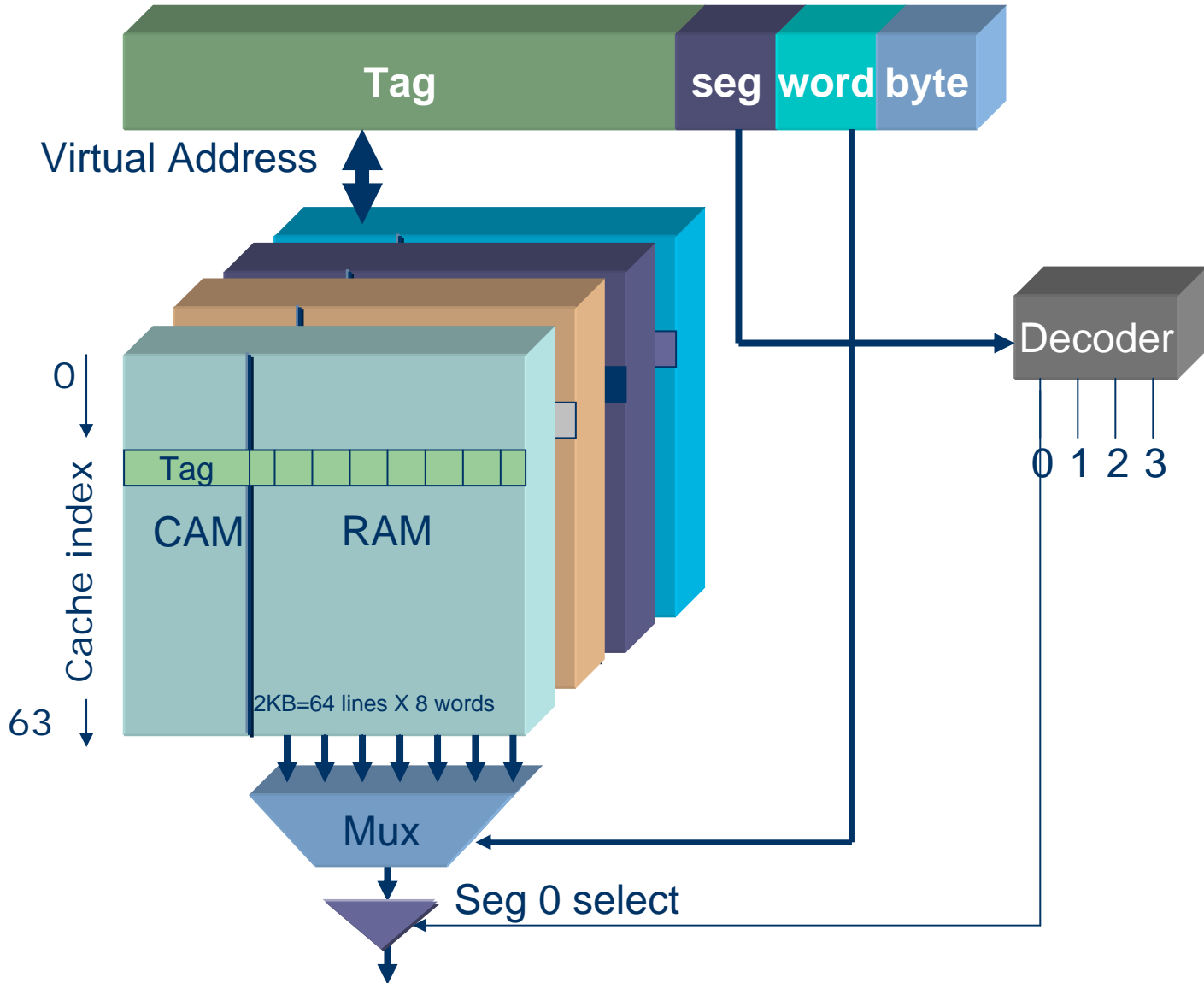
MMU

- Mapping sizes 1MB (Section), 64 KB (large page), 4KB (Small Page), 1KB (Tiny Page)
- 64 entries for both TLBs (Translation Look aside buffer)
- Round robin replacement

Cache and Write Buffer



Cache Organisation



Memory Management Unit (MMU)

Functions of MMU

- Virtual address to physical address translation
- Checking access permissions
- Two Levels of Tables for translating virtual address to physical address

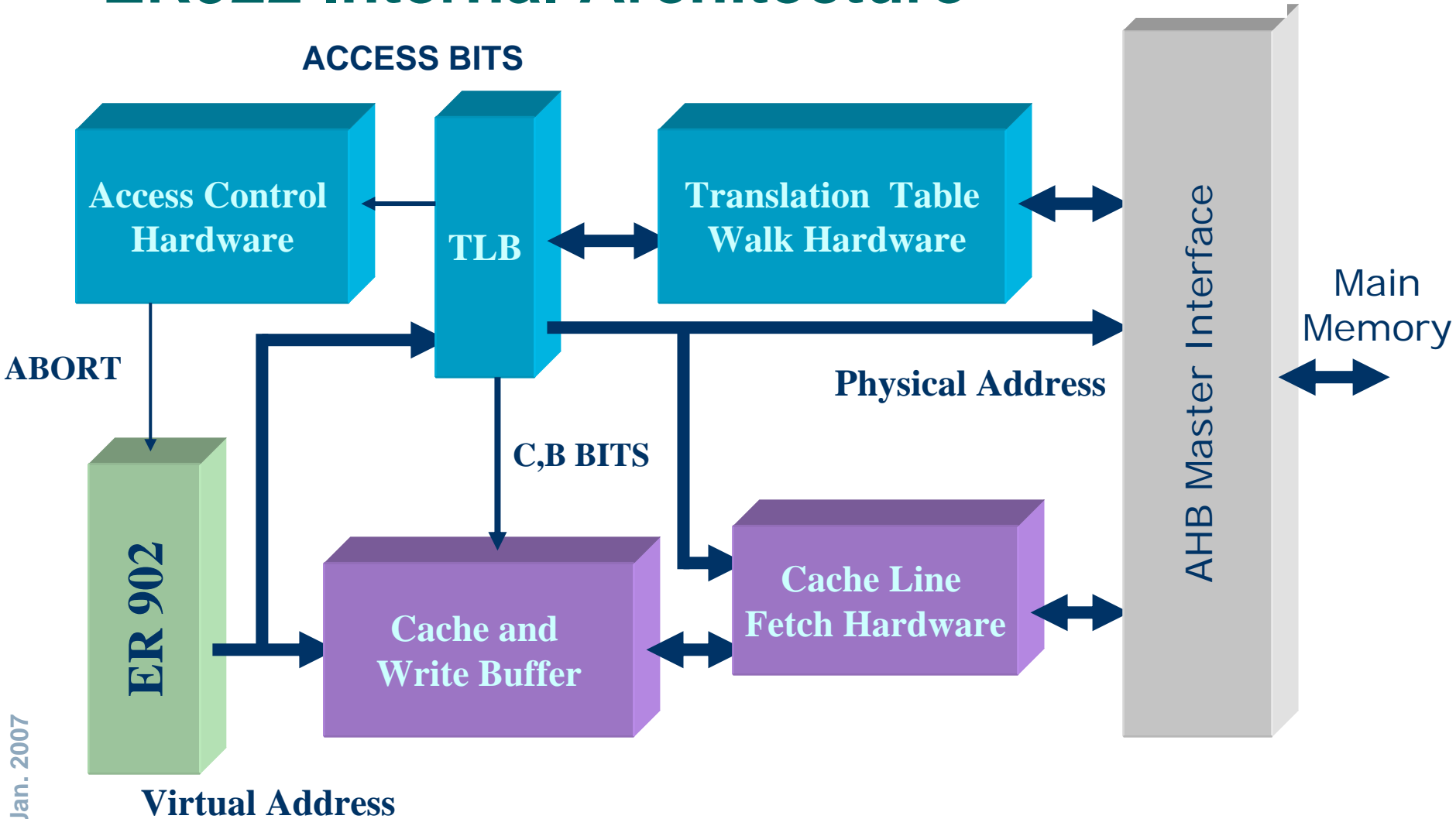
First-Level table:

Holds both section and pointer to Second-Level table

Second-Level table:

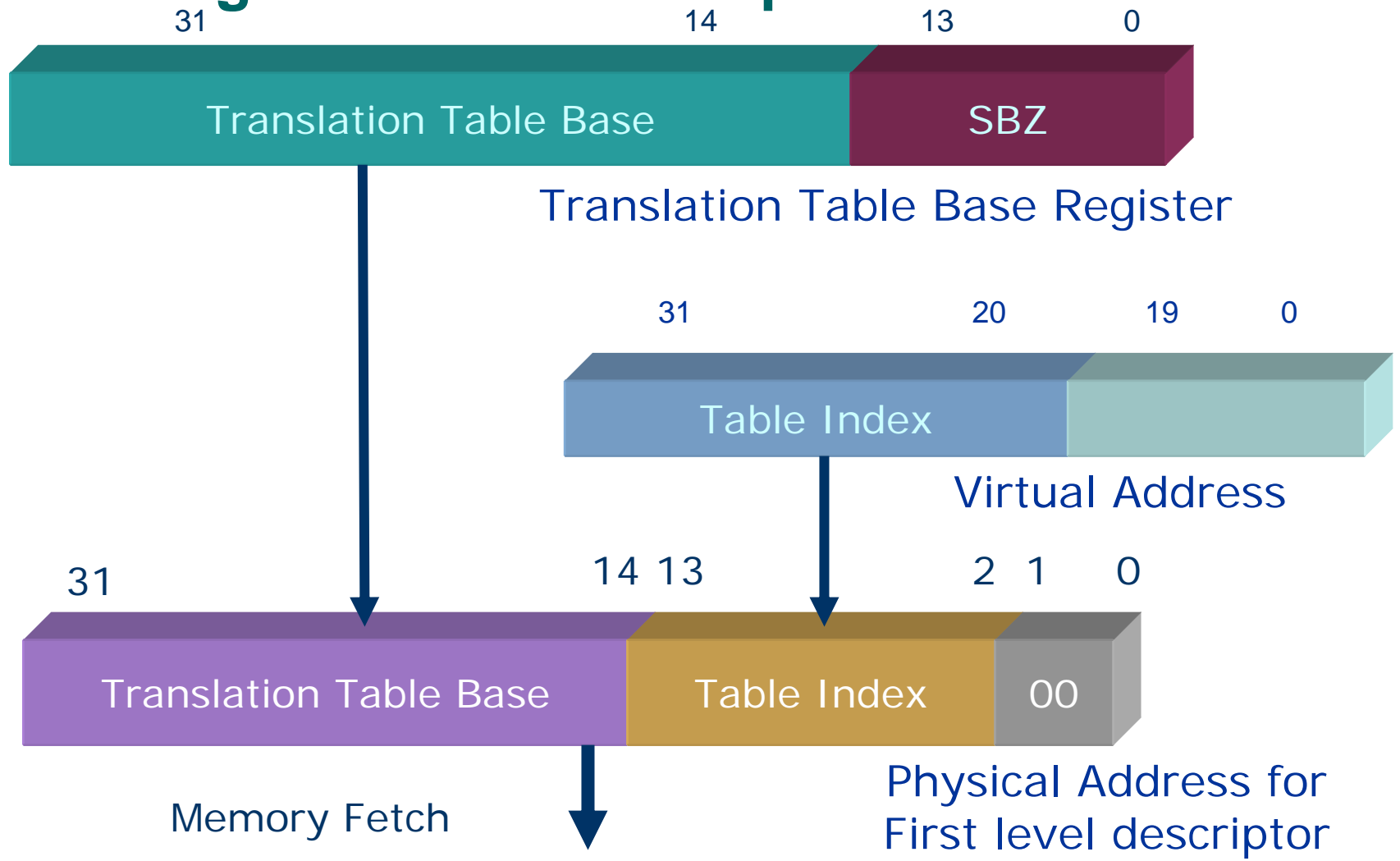
Holds both large and small page translation

ER922 Internal Architecture

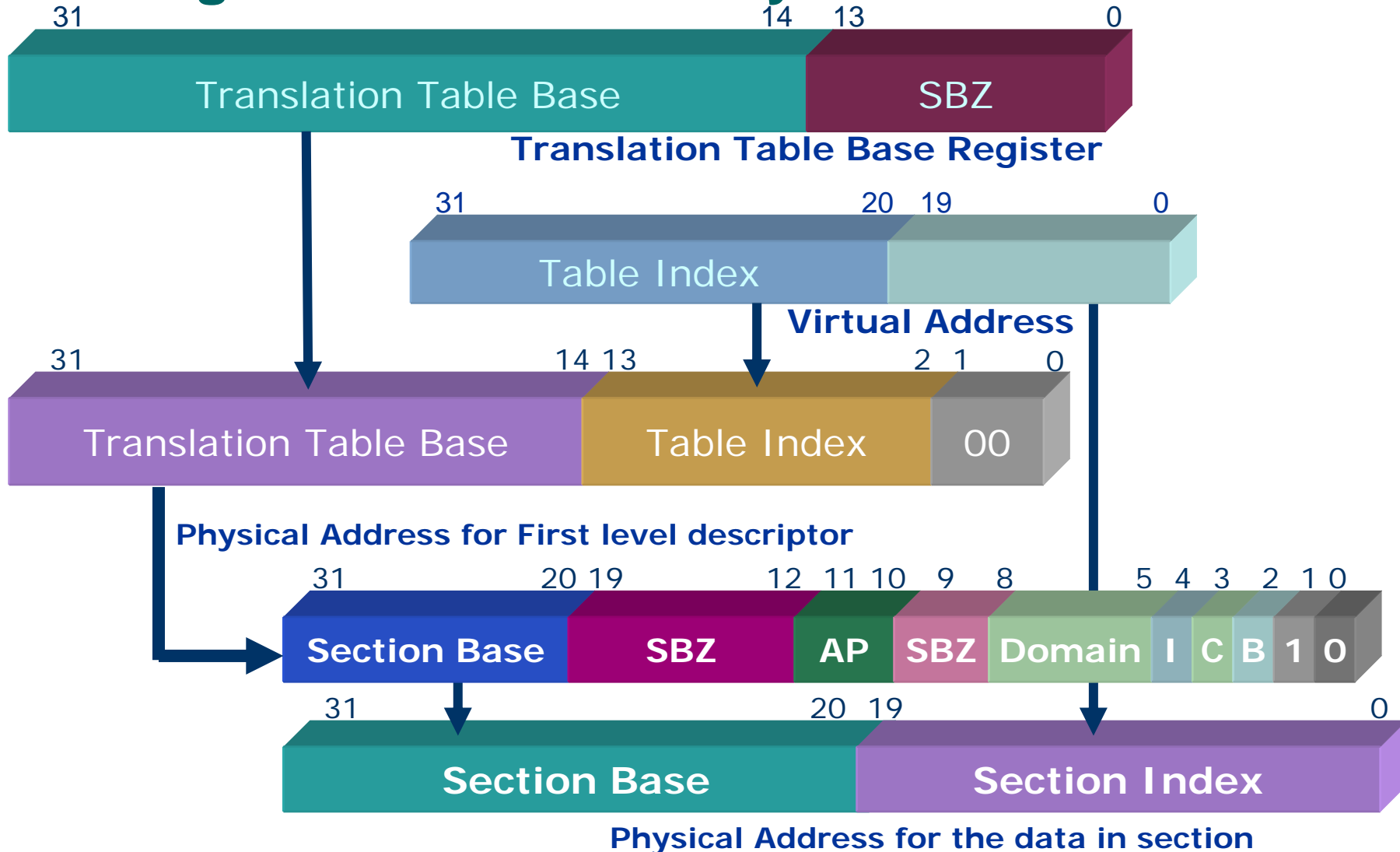


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Accessing First level Descriptor



Accessing a data from Memory in section



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ER902 based SoC Solutions

- BMI Processor Board (BMIPB)
- Digital Programmable Hearing Aid (DPHA)

BMI Processor Board

Interface Biomedical Instruments such as ECG, BP Monitor etc., with IBM compatible PC.

Key Features

- XC3S1500 - 1.5 Million gate FPGA
- Embedding in-house designed IP:
 - ER902 - 32-bit RISC Processor
 - ERUSB2 - USB2.0 Function Controller
 - ER16450 - UART
- 64 KB Flash EPROM
- 128 KB NVRAM
- Battery backed Real Time Clock
- 8 channel 12-bit ADC
- Two 32-bit Timers
- Interrupt Controller with 4-internal & 4-external sources
- RS-232 Port
- USB Port

BMI Processor Board (contd..)

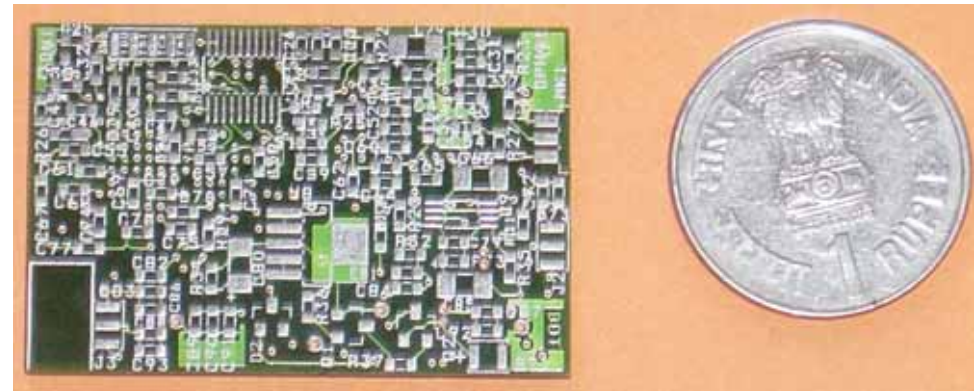
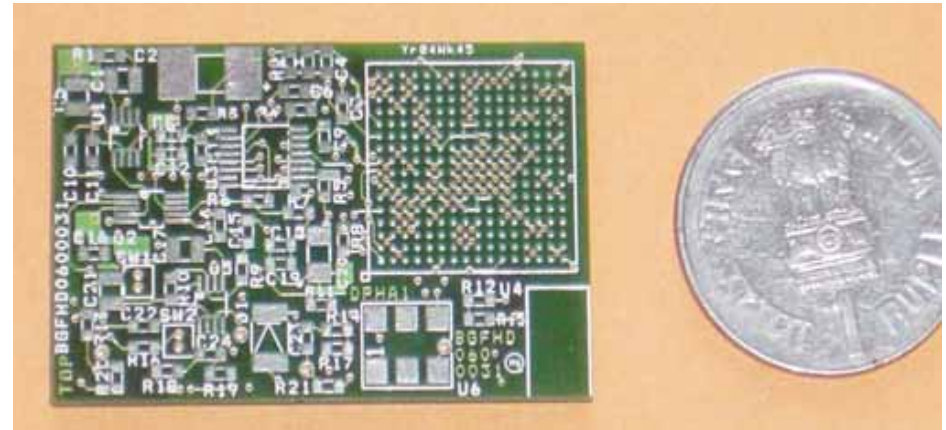


Top



Bottom

Digital Programmable Hearing Aid



Q & A

Thank you